Customer No.: 31561
Docket No.: 11955-US-PA
Application No.: 10/708,371

AMENDMENT

In The Claims:

Claim 1 (currently amended) A power amplifier with an active bias circuit, comprising:

a power amplifier transistor with a gate connected to a gate bias voltage; and

an active bias circuit ~~connected to~~ serially connected between an input power terminal of the power amplifier and the gate of the power amplifier transistor for receiving an input power from the input power terminal and outputting the gate bias voltage to the gate, wherein the gate bias voltage is increased corresponding to an increase of the input power, wherein the active bias circuit comprises a voltage source other than the input power.

Claim 2 (original) The power amplifier of claim 1, wherein a curve of an increase of the gate bias voltage versus the input power is a linear curve.

Claim 3 (original) The power amplifier of claim 1, wherein a curve of an increase of the gate bias voltage versus the input power is a non-linear curve.

Claim 4 (original) The power amplifier of claim 1, wherein the power amplifier transistor and the active bias circuit is manufactured by a system on chip (SOC) process.

Claim 5 (original) The power amplifier of claim 1, where the active bias circuit comprises a diode and a resistor.

Claim 6 (original) The power amplifier of claim 5, wherein an equivalent resistance of the diode in the active bias circuit varies in correspondence with the input power.

Claim 7 (currently amended) An integrated circuit for a power amplifier with an active bias circuit, comprising:

a power output device, from which a power is received for the power amplifier operation;

a power amplifier transistor with a gate connected to a gate bias voltage;

an active bias circuit ~~connected to~~ serially connected between the power output device and the gate of the power amplifier transistor for receiving an input power from the power output device and providing a gate bias voltage to the gate, wherein the gate bias voltage is increased corresponding to an increase of the input power, wherein the active bias circuit comprises a voltage source other than the input power; and

a power input device connected to an output terminal of the power amplifier transistor for receiving an amplified output power from the power amplifier transistor.

Claim 8 (original) The integrated circuit of claim 7, wherein a curve of an increase of the gate bias voltage versus the input power is a linear curve.

Claim 9 (original) The integrated circuit of claim 7, wherein a curve of an increase of the gate bias voltage versus the input power is a non-linear curve.

Claim 10 (original) The integrated circuit of claim 7, wherein the power amplifier transistor and the active bias circuit is manufactured by a system on chip (SOC) process.

Claim 11 (original) The integrated circuit of claim 7, wherein the power amplifier transistor and the active bias circuit is manufactured by a system on chip (SOC) process.

Claim 12 (original) The integrated circuit of claim 11, wherein the equivalent resistance of the diode in the active bias circuit varies in correspondence with the input power.

Claim 13 (currently amended) A method for generating a gate bias voltage of a power amplified transistor corresponding to an input power, comprising:

providing an input power to an active bias circuit disposed before the power amplified transistor; and

outputting a gate bias voltage corresponding to the input power, wherein the gate bias voltage is powered by a voltage source other than the input power and increased corresponding to an increase of the input power,

wherein the input power is transmitted along a path constituting of a first terminal from which the input power is inputted, the active bias circuit, the power amplified transistor, a terminal from which the gate bias voltage is outputted in that sequence.

Claim 14 (original) The method of claim 13, wherein a curve of an increase of the gate bias voltage versus the input power is a linear curve.

Claim 15 (original) The method of claim 13, wherein a curve of an increases of the gate bias voltage versus the input power is a non-linear curve.

Claim 16 (previously presented) The power amplifier of claim 1, wherein the active bias circuit comprises a grounded level.

Claim 17 (previously presented) The method of claim 7, wherein the active bias circuit comprises a grounded level.